Claims:

1. **A method for manufacturing, forming or creating** at least one dielectrically insulating trench (10) comprising rounded edges (14) of active silicon layer portions (6,7;3)adjacent to the trench, each of said rounded edges (14) located at a respective transition area (14) connecting to a buried insulating layer (2) of an SOI structure, said method comprising

   performing an etch process consisting of two steps, wherein

   - in the first step of the etch process said trench (10) is etched to the insulating layer (2);
   - in the second step of the etch process under-etched regions (12) are formed on (both) sidewalls of the trench (10) by isotropically etching a part of the insulating layer (2);

   after performing said etch process thermally oxidising surfaces of said trench (10) and said under-etched regions (12).

2. The method of claim 1, wherein said insulating layer (2) is used as an etch stop layer during said first step.

3. The method of claims 1 or 2, wherein in said second step a material removal at both sidewalls of the at least one trench (10) is small due to a selectivity of the isotropic etching, thereby substantially not resulting in a rounding of upper and lower edges of the trench (10).

4. The method of claim 3, wherein the material removal at the respective two sidewalls (10b) does not result in a rounding of upper and lower edges of the trench (10) and is substantially zero.

5. The method of claim 1 or 2, wherein the thermal oxidation is performed for creating the insulating layers (13) on the vertical walls (10a) of the isolation trench (10) and on surfaces (10b) of the under-etched regions (12).

6. The method of claim 1, wherein the buried insulating layer (2) is an SiO_2 layer.

7. **A method for creating** dielectric insulating trenches comprising rounded edges (14) of active silicon layer portions (6,7) at a transition area or at the respective transition area connecting to a buried insulating layer (2) of an SOI structure, comprising

after etching at least one of the isolation trenches (10), isotropically etching said buried insulating layer (2) so as to form under-etched regions (12) in the buried insulating layer (2); and

subsequently performing a thermal oxidation for creating an insulating layer (13) on vertical walls (10a) of the isolation trench (10) and in particular also on surfaces (10b) of the under-etches regions (12) so as to form rounded edges (14) of the insulating layers (13) above the edges (15) in the transition areas.

8. The method of claim 7, wherein the buried insulating layer is a SiO_2 layer.

9. The method of claims 7 or 8, wherein during the isotropic etching a material removal at the respective two sidewalls does not result in a rounding at upper and lower edges of the trench (10) and is substantially zero.

10. **SOI wafer** comprising at least one and preferably a plurality of dielectrically insulating trenches (10) having rounded edges (14) formed of active silicon layer portions (6,7;3) located adjacent to the trench, said rounded edges (14) located at a respective transition area (14) connecting to a buried insulating layer (2), said SOI wafer formed or being formable according to any of the preceding methods.

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